

METHOD OF FABRICATING FLASH MEMORY DEVICES

Abstract of the Disclosure

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A method of fabricating split gate type FLASH memory device comprises forming trench device isolation layers in a substrate to define a plurality of parallel first active regions. A gate insulation pattern, a conductive pattern and a hard mask pattern, which are sequentially stacked, are formed to have sidewalls aligned to sidewalls of the trench device isolation layer. Along 10 each of the first active regions, the hard mask pattern is removed at regular intervals to expose a top of the conductive pattern. An oxide pattern is formed on the exposed top of the conductive pattern and the hard mask pattern is removed. Using the oxide pattern as an etch mask, the conductive pattern is 15 etched to form floating gate patterns arranged over each of the first active regions at regular intervals. Tunnel oxide layers are formed on sidewalls of the floating gate patterns. A plurality of control gate electrodes are formed to cross over the first active regions. The control gate electrodes are disposed on the floating gate patterns.